



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,961	12/27/2001	Young Hun Ha	8733.524.00	7359
30827	7590	10/08/2004	EXAMINER	
MCKENNA LONG & ALDRIDGE LLP			LANDAU, MATTHEW C	
1900 K STREET, NW			ART UNIT	
WASHINGTON, DC 20006			PAPER NUMBER	
			2815	

DATE MAILED: 10/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/026,961

Applicant(s)

HA ET AL.

Examiner

Matthew Landau

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) 10-14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9, 15-18 and 20-22 is/are rejected.
- 7) ☒ Claim(s) 19 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9, 20, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Han et al. (US Pat. 5,926,235, hereinafter Han).

In regards to claim 1, Figures 4 and 5I of Han disclose a liquid crystal display device including a data line 115 supplied with a data signal, a gate lines 117 supplied with a scanning signal, a pixel electrode 104 for driving a liquid crystal cell, and a thin film transistor for responding to the scanning signal to switch the data signal to the pixel electrode, the device comprising: a storage electrode 130 overlapping with the gate line to form a storage capacitor; a first protective layer 113a being formed between the storage electrode and the pixel electrode at a portion of an overlapping area between the storage electrode and the pixel electrode (portion over the right side of the storage electrode, as shown in Figure 5I), wherein the storage electrode is directly connected to the pixel electrode at an end of the overlapping area (Figure 5I); and a second protective layer 113a formed between a gate insulating film 109 and the pixel electrode.

In regards to claim 2, Figure 5I of Han discloses the gate insulating film 109 on a substrate 110 in such a manner to cover the gate line; and a first semiconductor layer 111/112 between the gate insulating film and the storage electrode.

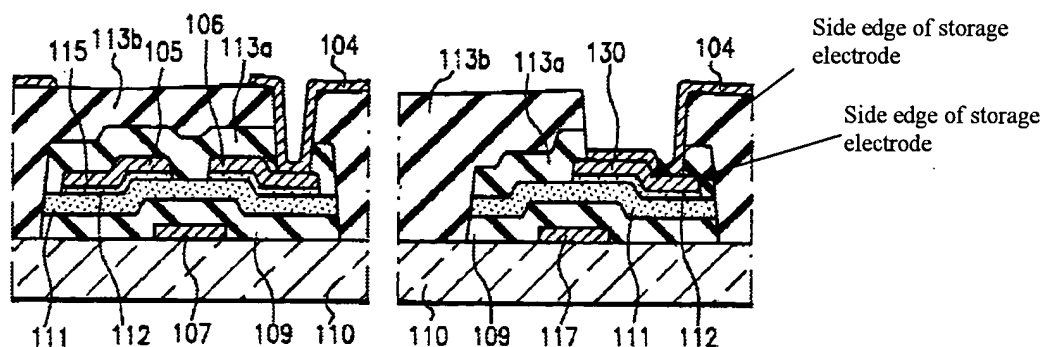
Art Unit: 2815

In regards to claim 3, Figure 5I of Han discloses the first protective layer 113a is formed at side edges of the storage capacitor (column 4, lines 28-32).

In regards to claim 4, Figures 4 and 5I of Han disclose a gate electrode 107 contacting the gate line 117 on the substrate 110; a second semiconductor layer 111/112 on the gate insulating film; and a source electrode 105 and a drain electrode 106 on the second semiconductor layer.

In regards to claims 5, 9, and 21, Figure 5I of Han discloses the second semiconductor layer 111/112 includes an active layer 111 and an ohmic contact layer 112. The limitations “the active layer is patterned simultaneously with...” and “the ohmic contact layer is patterned simultaneously with...” are product-by-process limitations that do not structurally distinguish the claimed invention over Han.

In regards to claim 6, Figures 4 and 5I of Han disclose a liquid crystal display device including a data line 115 supplied with a data signal, a gate lines 117 supplied with a scanning signal, a pixel electrode 104 for driving a liquid crystal cell, and a thin film transistor for responding to the scanning signal to switch the data signal to the pixel electrode, the device comprising: a storage electrode 130 overlapping the gate line to form a storage capacitor; and the pixel electrode covering an upper surface and side edges of the storage electrode, wherein the storage electrode is directly connected to the pixel electrode at an end of an overlapping area between the storage electrode and the pixel electrode. A marked-up version of Figure 5I is provided below for clarification.



Art Unit: 2815

In regards to claim 7, Figures 4 and 5I of Han disclose the gate line 117 formed on a substrate 110; a gate insulating film 109 formed on the substrate to cover the gate line; and a first semiconductor layer 112 formed on the gate insulating film. The product-by-process limitations “simultaneously patterned with the storage electrode” does not structurally distinguish the claimed invention over Han.

In regards to claim 8, Figures 4 and 5I of Han disclose a gate electrode 107 connected with the gate line 117 on said substrate 110; a gate insulating film 109 on said substrate; a second semiconductor layer 111/112 on said gate insulating film; a source electrode 105 and a drain electrode 106 on said second semiconductor layer; a protective layer 113a on said gate insulating film; and the pixel electrode 104 on said protective layer.

In regards to claim 20, the product-by-process limitation “wherein the first protective layer is simultaneously formed...” does not structurally distinguish the claimed invention over Han.

Claims 1-4, 6-8, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (US Pat. 6,091,466, hereinafter Kim).

In regards to claim 1, Figures 4 and 5F disclose a liquid crystal display device including a data line 123 supplied with a data signal, a gate lines 113 supplied with a scanning signal, a pixel electrode 141 for driving a liquid crystal cell, and a thin film transistor for responding to the scanning signal to switch the data signal to the pixel electrode, the device comprising: a storage electrode 151 overlapping with the gate line to form a storage capacitor; a first protective layer 137 being formed between the storage electrode and the pixel electrode at a portion of an

Art Unit: 2815

overlapping area between the storage electrode and the pixel electrode (portion over left portion of storage electrode, as shown in Figure 5F), wherein the storage electrode is directly connected to the pixel electrode at an end of the overlapping area; and a second protective layer 137 formed between a gate insulating film 117 and the pixel electrode (portion of 137 between drain electrode 131 and pixel electrode 141). As shown in Figure 5F of Kim, the pixel goes through the storage electrode, essentially forming a hole in the middle of the storage electrode (contact hole 181). This hole can be considered “an end of the overlapping area” since the pixel and storage electrodes are no longer overlapping at this point. The pixel electrode 141 and the storage electrode 151 are directly connected in the hole. Therefore, the claim is anticipated.

In regards to claim 2, Figure 5F of Kim discloses the gate insulating film 117 on a substrate 101 in such a manner to cover the gate line; and a first semiconductor layer 133a/135a between the gate insulating film and the storage electrode.

In regards to claim 3, Figure 5F of Kim discloses the first protective layer 137 is formed at side edges of the storage capacitor.

In regards to claim 4, Figures 4 and 5F of Kim disclose a gate electrode 111 contacting the gate line 117 on the substrate 101; a second semiconductor layer 133/135 on the gate insulating film; and a source electrode 121 and a drain electrode 131 on the second semiconductor layer.

In regards to claim 6, Figures 4 and 5F of Kim disclose a liquid crystal display device including a data line 123 supplied with a data signal, a gate lines 113 supplied with a scanning signal, a pixel electrode 141 for driving a liquid crystal cell, and a thin film transistor for responding to the scanning signal to switch the data signal to the pixel electrode, the device

Art Unit: 2815

comprising: a storage electrode 151 overlapping with the gate line to form a storage capacitor; the pixel electrode 141 covering an upper surface and side edges of the storage electrode (Figure 5F), wherein the storage electrode is directly connected to the pixel electrode at an end of an overlapping area between the storage electrode and the pixel electrode (see rejection of claim 1).

In regards to claim 7, Figures 4 and 5F of Kim disclose the gate line 113 formed on a substrate 101; a gate insulating film 117 formed on the substrate to cover the gate line; and a first semiconductor layer 135a formed on the gate insulating film. The product-by-process limitations “simultaneously patterned with the storage electrode” does not structurally distinguish the claimed invention over Kim.

In regards to claim 8, Figures 4 and 5F of Kim disclose a gate electrode 111 connected with the gate line 113 on said substrate 101; a gate insulating film 117 on said substrate; a second semiconductor layer 133/135 on said gate insulating film; a source electrode 121 and a drain electrode 131 on said second semiconductor layer; a protective layer 137 on said gate insulating film; and the pixel electrode 141 on said protective layer.

In regards to claim 20, the product-by-process limitation “wherein the first protective layer is simultaneously formed...” does not structurally distinguish the claimed invention over Kim.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

Art Unit: 2815

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 15-18 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han in view of Kim (US Pat. 6,262,784).

In regards to claim 15, Figures 4 and 5I of Han disclose a first substrate 110; a gate line 117 and a data line 115 over the substrate, the data line crossing the gate line to define a pixel region; a thin film transistor having source and drain electrodes (105 and 106) at the crossing of the gate line and data line; a storage electrode 130 over the gate line; a pixel electrode 104 over the storage electrode; a first protective layer 113a patterned on a central portion of an overlapping area of the storage electrode between the storage electrode and the pixel electrode, wherein the pixel electrode directly connects to the storage electrode at an end of the overlapping area between the storage electrode and the pixel electrode; a second protective layer 113b formed between a gate insulating film 109 and the pixel electrode. Han does not explicitly disclose a second substrate with a liquid crystal layer between the first and second substrates. Figure 3 of Kim discloses a liquid crystal layer 190 formed between first and second substrates (100 and 200). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Han for the purpose obtaining a fully functional liquid crystal display device.

In regards to claim 16, Figure 4 of Han discloses a pixel electrode 104 of an adjacent pixel region extends over the storage electrode 130.

In regards to claim 17, Figure 5I of Han discloses a storage capacitor is formed between the storage electrode 130 and the gate line 117 and wherein the first protective layer 113a overlaps a portion of the storage capacitor.



Art Unit: 2815

In regards to claim 18, Figure 5I of Han discloses a storage capacitor is formed between the storage electrode 130 and the gate line 117 and wherein the first protective layer 113a overlaps a lower edge of the storage capacitor.

In regards to claim 22, the product-by-process limitation “wherein the first protective layer is simultaneously formed...” does not structurally distinguish the claimed invention over the prior art.

#### *Allowable Subject Matter*

Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including the pixel electrode of the adjacent pixel region is substantially rounded where the pixel electrode of the adjacent pixel region extends over the storage electrode.

#### *Response to Arguments*

Applicant's arguments filed August 3, 2004 have been fully considered but they are not persuasive.

In response to Applicant's arguments that Han fails to teach or suggest “a first protective layer formed between the storage electrode and the pixel electrode at a portion of an overlapping

Art Unit: 2815

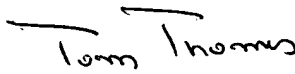
area between the storage electrode and the pixel electrode, wherein the storage electrode is directly connected to the pixel electrode at an end of the overlapping area between the storage electrode and the pixel electrode”, Han discloses all the limitations of claim 1 as explained in the above rejection.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

  
TOM THOMAS  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800

Matthew C. Landau

Examiner

October 6, 2004